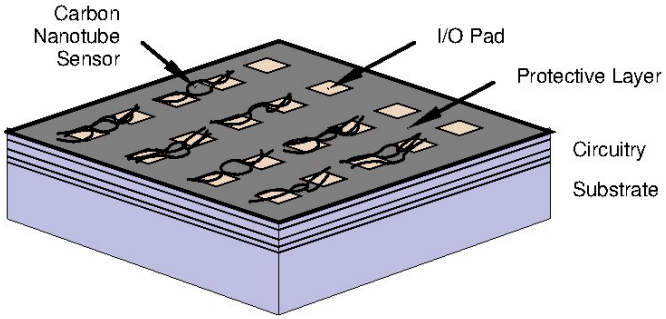
One Chip, Millions of Nanocontrollers

Although people often think of the primary contributions of computer technology as being PCs, the Internet, or supercomputing for "grand challenge" problems, by far the most direct impact of computer technology on society has been the ability to make a wide range of ordinary devices "intelligent." Programmable control is everywhere – except in devices that are too small to fit a microcontroller. The NANOCONTROLLERS we propose require orders of magnitude less circuitry, enabling nanocontrollers to fit alongside or under the devices they control.

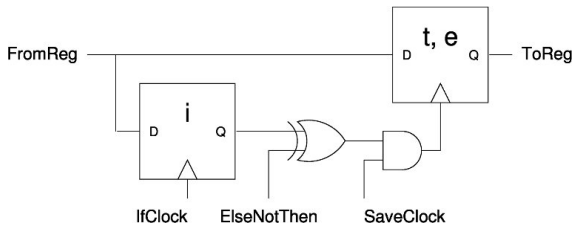


For example, chemical or biological single-chip sensor arrays (as shown in the above figure) use small electrical changes in carbon nanotubes to detect and measure the levels of a wide range of chemical and biological toxins; a million-sensor chip would naturally output a million weak analog signals to be decoded elsewhere. Placing a nanocontroller *under each sensor* not only allows calibrated correction of sensor defects in software, but also would allow data to be directly output as digital PPM concentrations of the toxins sensed – or even as digitized audio messages saying what protective gear is needed.

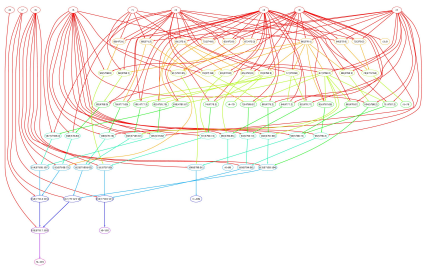
Not all nanocontroller applications are controlling physically small devices; for example, large programmable sheets of printed organic semiconductor materials offer equally impressive possibilities. To enable these and other applications, nanocontrollers must have the following properties:

- **Minimal Circuit Size**: no more than a few hundred transistors per nanocontroller
- **Predictable Real-Time Behavior**: computations must meet real-time control constraints
- **Localized Input/Output**: each nanocontroller must talk with the device it controls
- **Coordination As A Parallel Computer**: nanocontrollers must work together to reduce external I/O to an acceptable level (e.g., summarizing sensed values rather than passing them all off-chip)
- **Each Nanocontroller Independently Programmable**: nanofabricated devices often have significant manufacturing variations that require individualized correction, perhaps even different algorithms
- **Reprogrammability**: it must be possible (but not necessarily fast) to reprogram a part to correct for defects that develop over time or to enhance functionality

The key to this is actually a compiler technology that allows millions of independent programs to be merged into a single state machine while preserving relevant timing properties. This technology, called **META-STATE CONVERSION (MSC)**, makes independent program memories unnecessary – *nanocontroller circuit complexity is not proportional to program complexity.* In combination with aggressive use of new compile-time optimization technologies (from gate-level logic optimization to a new genetic algorithm for code ordering and register allocation) and a very simple 1-bit datapath, digital nanocontrollers require at most a few hundred transistors; switched-analog nanocontrollers might be feasible using just a few dozen transistors. A digital nanocontroller consists of tens of 1-bit registers and the logical equivalent of a 1-of-2 input multiplexor:



Even simple computations require many 1-bit multiplexor operations. For example, squaring an 8-bit integer yields the DAG:



There has been good progress on nanocontrollers over the past year, with two M.S. theses completed on the topic in 2010. Shashi Deepa Arcot's thesis describes *Genetic Algorithm Controlled Common Subexpression Elimination for Spill-Free Register Allocation*, an important component of the compilation toolchain. In contrast, Akshay Vummannagari 's thesis, *Verilog Design and FPGA Prototype of a Nanocontroller System*, presents the first complete specification of the digital hardware. However, there is still much to be done.

In 2012, we have started working toward building a nanocontroller-based large-format image sensor. Nominally, our sensor design target is 500MP with HDR (high dynamic range) full-frame capture at 1,000 FPS equivalent or more. That would be an infeasible 1TB/s if the data was not compressed on chip....

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