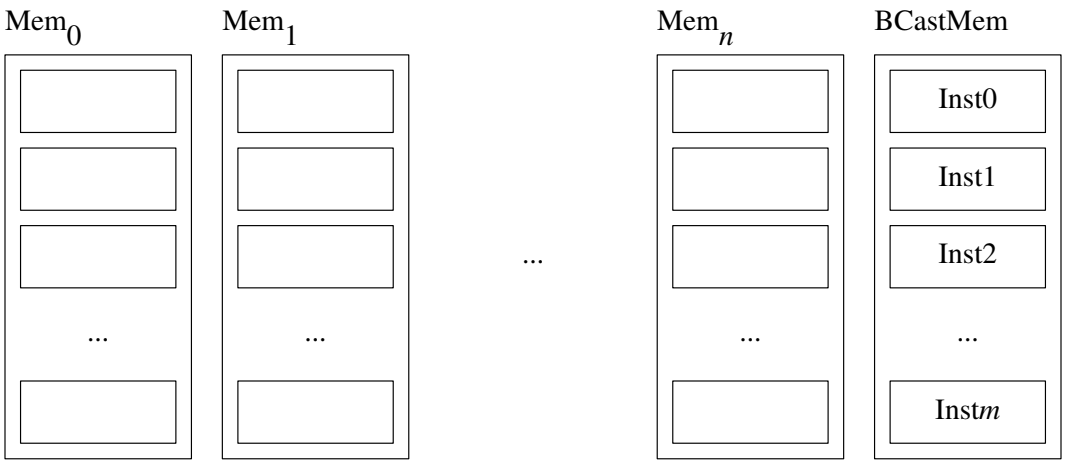

Figure 3: Memory Layout For SIMD Execution