

EE480 Fall 2016 Exam 0

Your name is:

Your email address is:

The question you skipped is:

There are 11 questions. Each of the questions is worth 10 points; you must answer any 10 and indicate above which one you skipped (no extra credit). For each question with boxes, ☐, in front of each potential answer, read the question carefully to see if you should check a single answer or all answers that apply. The short answer questions should get **short** answers; excessively long answers may be considered incorrect. The test is without calculators, closed book, closed notes, closed minds (no reading your neighbor's mind nor test paper ;-).

1. For this question, mark all answers that apply. Which of the following statements are consistent with the following AIK specification:

```

jump t .a := 3:2 .a:14
jump f .a := 2:2 .a:14
push .a := 1:2 .a:14
.op := 0:2 .this:14
.alias .op { 0 add afp and asp call div ind mark mul
               neg or pop release ret store sys test xor }

```

- ☐ **push 1+4** would be encoded as 0x4005
 - ☐ The instruction encoded as 0x0001 would be **afp**
 - ☐ A line of assembly language input like **.origin 0x0010** is nonsense
 - ☐ The number of bits used to encode an instruction depends on the instruction
 - ☐ Instructions are encoded such that there is an argument only if the 2 most significant bits are not both 0
2. In class, we talked about assemblers using multiple passes. What problem are multiple passes trying to resolve? Give an example using the instruction set described in the previous question.

3. For this question, mark all answers that apply. Which of the following Verilog expressions results in a value of 1 (decimal)?

- ☐ `4'b0001`
- ☐ `(4'bxxxx === 1'hx)`
- ☐ `{1'b1, 1'b0}`
- ☐ `a where or(a, 0, 1);`
- ☐ `a[1] where reg [1:0] a = 2;`

4. For this question, mark all answers that apply. Which of the following statements about Verilog are true?

- ☐ The `=` operator can be used to assign a value to a **wire**
- ☐ You cannot mix **reg** and **wire** values within a statement
- ☐ `#42` would be specifying a delay of 42 simulated-time units
- ☐ The Verilog **if** construct can be used in synthesizable code
- ☐ Given `reg [31:0] a[0:1];`, `a[0]` would be the first of two 32-bit elements in **a**

5. Briefly explain what **line** and **toggle coverage** refer to. Does 100% coverage by either of those methods guarantee that every possible error will be detected?

9. What is **\$dumpvars** used for?
10. Without using any Verilog comparison operators, write a synthesizable **module less(lessout, ain, bin)** that returns 1 for **lessout** only if the two-bit unsigned value **ain** is less than the two-bit unsigned value **bin**.

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11. Write an exhaustive **module testbench** for the module **ha** given below, which implements a half adder.

```
module ha(sum, cout, a, b);  
output sum, cout;  
input a, b;  
xor(sum, a, b);  
and(cout, a, b);  
endmodule
```